AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions, and listing, of claims in the application:

Listing of Claims

1.-8. (Canceled without Prejudice)

9. (Currently Amended) A method of translating a voltage level of a single-ended input signal using a single ended input circuit having at least one native NMOS transistor device having a threshold voltage less than 0V and a gate that is grounded, said method comprising:

outputting a first voltage level if the single ended input signal is in a first state; and

outputting a second voltage level if the single ended input is in a second state.

10. (Original) The method of Claim 9, wherein said first state comprises a high state.

11. (Original) The method of Claim 9, wherein said second state comprises a low state.

12. (Original) The method of Claim 9, wherein said first voltage level comprises a high signal.

13. (Original) The method of Claim 9, wherein said second voltage level comprises a low signal.

14. (Original) The method of Claim 9, wherein said first voltage level comprises a low signal.

15. (Original) The method of Claim 9, wherein said second voltage level comprises a high signal.

16. (Currently Amended) A method of translating a voltage level of a single-ended input signal using a single ended input circuit having at least one native NMOS transistor device having a threshold voltage less than 0V and a gate that is grounded, said method comprising:

determining if the input signal is high;

outputting a low signal if the input signal is high; and

outputting a high signal if the input signal is not high.

17. (Original) The method of Claim 16, wherein determining if the input signal is high comprises determining if the input signal is greater than a first voltage.

18. (Original) The method of Claim 16, wherein determining if the input signal is not high comprises determining if the input signal is less than a second voltage.

19. (Original) The method of Claim 16, further comprising eliminating static current drain.

20. (Previously Presented) A method of translating a voltage of an input signal from one level to another level using at least one level shifter circuit having a single ended input, said level shifter circuit including a first native NMOS transistor device having a threshold less than OV, a second transistor device coupled to the first native transistor device and a level shifter circuit coupled to at least the first native and second transistor devices comprising:

determining if the input signal is greater than a threshold value of said second NMOS transistor device;

outputting a low signal if the input signal is greater than said threshold value;

outputting a high signal if the input signal is not greater than said threshold value; and

eliminating static current drain.

21. (Previously Presented) The method of claim 20 wherein outputting a low signal comprises pulling an output signal to ground.

22. (Previously Presented) The method of claim 20 wherein outputting a high signal comprises determining if the input signal is greater than a second threshold value.

23. (Previously Presented) The method of claim 22 wherein outputting a high signal comprises pulling an output signal to VDD.

24. (Previously Presented) The method of claim 22 comprising determining if the input signal is less than the threshold value of said second NMOS transistor device but greater than said second threshold.

25. (New) A method of translating a voltage level of an input signal using a circuit having at least one native NMOS transistor device having a gate that is grounded, said method comprising:

outputting a first voltage level if the input signal is in a first state; and

outputting a second voltage level if the single ended input is in a second state.

26. (New) An input level shifter circuit, said input level shifter circuit comprising:

an input signal; and

a native NMOS transistor, said native NMOS transistor further comprising:

a source that is electrically coupled to the input signal; and

a gate that is grounded.